changes prior to exciting of successive gate signal lines, wherein the first gate voltage has a voltage level that turns on the switching transistor. For example only, and not by way of limitation, Applicant points the Examiner's attention to the embodiment described with respect to Figs. 5 and 6, where it can be seen that the gate driver 34 receives first (V_{GH}) and second (V_{GL}) gate voltages, wherein the first gate voltage (V_{GH}) changes from V_{DD} to GVL at the falling edge of the gate scanning clock signal GSC prior to exciting the successive gate line at the next rising edge of GSC (see Fig. 6).

Yasui et al. clearly lacks such a feature. As shown in Fig. 2 of Yasui et al., for example, the first gate voltage in Yasui et al. corresponds to V_{GH}, the voltage level of the high-level gate pulse P_G. Applicant respectfully submits that the Examiner has failed to cite any disclosure or suggestion in Yasui et al. that the first gate voltage V_{GH} changes prior to exciting of successive gate signal lines. Indeed, Figs. 2, 4A-B, 5A-B, 8A-D, etc. of Yasui et al. all indicate that the gate driver 3 merely switches from providing the first gate voltage V_{GH}, to providing the second gate voltage V_{GL}, coincident with, or prior to, exciting successive gate signal lines (see also col. 15, lines 1-14).

Accordingly, Yasui et al. cannot possibly anticipate the invention of claim 1 under 35 U.S.C. § 102(e). Therefore, Applicant respectfully requests that the Examiner withdraw his rejection and allow claim 1.

Claim 7

Claim 7 recites a method of driving an active matrix liquid crystal display apparatus which includes, among other things, a step of supplying a first gate voltage and a second gate voltage, selectively via a switching device, to the gate lines, said switching device being controlled by a shift register, wherein the first gate voltage varies before the second gate voltage

is supplied to the gate lines. For example only, and not by way of limitation, Applicant again points the Examiner's attention to the embodiment described with respect to Figs. 5 and 6, where it can be seen that the switching device 39 receives first (V_{GH}) and second (V_{GL}) gate voltages, wherein the first gate voltage (V_{GH}) varies from V_{DD} to GVL by means of switch 50 at the falling edge of the gate scanning clock signal GSC before the second gate voltage (V_{GL}) is supplied to the gate line by the switch 39.

Yasui et al. clearly lacks such a feature. As shown in Fig. 2 of Yasui et al., for example, the first gate voltage corresponds to V_{GH}, the voltage level of the high-level gate pulse P_G, and the second gate voltage corresponds to V_{GL}. Applicant respectfully submits that the Examiner has failed to cite any disclosure or suggestion in Yasui et al. that the first gate voltage V_{GH} varies before the second gate voltage V_{GL} is applied to the gate line. Indeed, Figs. 2, 4A-B, 5A-B, 8A-D, etc. of Yasui et al. all indicate that the gate driver 3 switches from the first gate voltage V_{GH} to the second gate voltage V_{GL} without providing for any variation in the first gate voltage V_{GH}.

Accordingly, Yasui et al. cannot possibly anticipate the invention of claim 7 under 35 U.S.C. § 102(e). Therefore, Applicant respectfully requests that the Examiner withdraw his rejection and allow claim 7.

Claims 8-9, dependent from claim 7, are deemed to be similarly allowable.

35 U.S.C. § 103

The Examiner rejected claims 2-6 under 35 U.S.C. § 103 as unpatentable over Yasui et al. in view of Suzuki et al. Applicant respectfully traverses those rejections for at least the following reasons.

Among other things, Suzuki et al., like Yasui et al, fails to disclose or suggest a gate driver receives a first gate voltage which changes prior to exciting of successive gate signal lines,

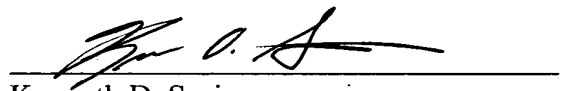
wherein the first gate voltage has a voltage level that turns on the switching transistor. Applicant respectfully submits that the Examiner has not stated that Suzuki et al. includes such an element, and indeed it does not. Accordingly, as at least this one element of the claimed invention is missing from both Suzuki et al. and Yasui et al, no possible combination of Suzuki et al. and Yasui et al can produce the present invention of claims 2-6 which includes such an element. Therefore, Applicant respectfully requests that the Examiner withdraw his rejections and allow claims 2-6.

In view of the foregoing, Applicants respectfully request that the application be reconsidered, that claims 1-9 be allowed, and the application pass to issue. Please charge any insufficiency or credit any overpayment to Deposit Account No. 50-0911.

Respectfully submitted,

LONG ALDRIDGE & NORMAN, LLP

Date: May 10, 2001



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